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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,903	10/30/2003	Harm Peter Hofstee	AUS920030403US1	9209

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EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,903	HOFSTEE ET AL.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 8-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita (US Patent Number 6,366,109) in view of Miller et al. (US Patent Number 4,292,668 hereinafter "Miller").

3. As per claims 8, 15 and 21 Matsushita teaches a method, system and product comprising,

one or more processors (processor, lines 40 – 44);

one or more interface pins (column 1, lines 43 – 45);

an interface controller (element 40, figure 1);

a memory accessible by the processors (memory, element 100, figure 4, column 6, lines 18 – 20);

one or more nonvolatile storage devices accessible by the processors (element 9, auxiliary storage such as hard disc drives, a floppy disc drive, etc, figure 1); and

an interface pin assignment tool for assigning one or more of the interface pins to the interface controller, the interface pin assignment tool including:

means for receiving a first assignment request (signal, element 44, figure 1);

means for identifying one or more of the interface pins that correspond to the first assignment request (address signal, element 46, figure 2); and

means for associating the identified interface pins with the selected interface controller (recognition decoder carries out means for associating, column 6, lines 9 – 23).

Matsushita discloses the I/O controller connected to multiple I/O devices but does not explicitly disclose a system having plurality of interface controllers; a means for selecting a first interface controller from the plurality of interface controllers that correspond to the first assignment request.

Miller analogously teaches a plurality of interface controllers (IOC, elements 206, 208, 210, 212, figure 1); and a means for selecting a first interface controller from the plurality of interface controllers that correspond to the first assignment request (selection of IOC based on selection of peripheral device requesting first assignment, column 14, lines 4 – 24).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify Matsushita with the above teachings of Miller such that it comprises a I/O Controller for a I/O device is needed to function appropriately. One of ordinary skill would have been motivated to make such modification in order to enable the function for a multitude of peripherals to interface via I/O Controllers and processor (column 7, lines 53 – 67, column 8, lines 1 – 10).

4. Matsushita modified by the teachings of Miller as applied in claims 8, 15 and 21 above, as per claims 9, 16 and 22 Matsushita teaches a method, system and product wherein the identified interface pins are selected from the group consisting of an input interface pin (physical pin, column 3, lines 27 – 32) and an output interface pin (outputs, column 7, lines 6 – 12).

5. Matsushita modified by the teachings of Miller as applied in claims 8, 15 and 21 above, as per claims 10, 17 and 23 Matsushita teaches a method, system and product comprising,

receiving a second assignment request, the second assignment request corresponding to the identified interface pins (different semiconductor devices, column 6, lines 58 – 67);

selecting a second interface controller from the plurality of interface controllers that correspond to the second assignment request (unit selecting, column 7, lines 56 – 61); and

re-associating the identified interface pins to the second interface controller (column 7, lines 59 – 61).

6. As per claims 11, 18 and 24 Matsushita teaches a method, system and product wherein the associating is performed using a look-up table (pin correspondence table, column 1, lines 26 – 34).

7. Matsushita modified by the teachings of Miller as applied in claims 8, 15 and 21 above, as per claims 12, 19 and 25 Matsushita teaches a method, system and product further comprising:

determining whether there are more interface pins that are not associated with the first interface controller (column 6, lines 45 –52); and

assigning the non-associated interface pins to a second interface controller in response to the determination (inactivated, column 6, lines 53 – 57).

8. As per claims 13, 20 and 26 Matsushita teaches a method, system and product comprising,

receiving data from the identified interface pins (input signal); and

providing the data to the first interface controller (input signal, element 62, figure 2, column 4, lines 45 – 49).

9. Matsushita modified by the teachings of Miller as applied in claims 8, 15 and 21 above, as per claims 14 and 27 Miller teaches a method and product wherein the associating is performed at system initialization (system startup/initialization sequence, figure 16).

Response to Arguments

10. Applicant's arguments filed 10/5/2006 have been fully considered but they are not persuasive. The Applicant argues:

1.) Date of Miller is over a quarter of a century old.

2.) Miller, other than teaching having more than one interface controller, does not teach or suggest any of the claimed limitations of receiving an assignment request, identifying interface pins that correspond to the assignment request, selecting a controller that corresponds to the assignment request nor associating the identified pins with the selected interface controller.

3.) Matsushita does not teach selecting an interface controller.

4.) Matsushita does not teach associating the identified interface pins with the selected interface controller.

5.) Applicant states that Examiner no longer contends that Matsushita's "recognition decoder" is analogous to the interface controller and holds that recognition decoder provides means for associating pins with the selected interface controller, however Matsushita does not teach associating any pins with a selected interface controller.

6.) Applicant states that Examiner admits Matsushita's shortcomings of not teaching selecting a first interface controller from the assignment request, and combines with Miller because Miller teaches a plurality of interface controllers however the combination does not render the applicant's claimed invention obvious.

11. As per argument 1, the Examiner respectfully disagrees. In response to applicant's argument based upon the age of the references, contentions that the reference patents are old are not impressive absent a showing that the art tried and

failed to solve the same problem notwithstanding its presumed knowledge of the references. See *In re Wright*, 569 F.2d 1124, 193 USPQ 332 (CCPA 1977).

12. As per argument 2, the Examiner respectfully disagrees. Examiner refers to rejection of claims 8, 15 and 21 above as seen in the previous Office Action. The purpose of combining Miller and Matsushita was to show that an I/O device is connected via an interface controller. Matsushita already teaches a plurality of I/O devices however does not explicitly mention the fact taught by Miller that an interface controller is present. The Examiner agrees with the applicant that the reference is nearly a quarter of a century old and such an age of a reference shows that one of ordinary skill in the art would recognize that an I/O device is connected to a system via an interface controller. The Examiner has not independently relied on Miller for the claim limitations stated above in argument 2 but in fact a combination of both Miller and Matsushita.

13. As per argument 3, the Examiner respectfully disagrees. The explanation the Applicant has provided on page 10 of the Remarks received on 10/5/2006, refer to selecting an interface controller. The Applicant states that the Examiner has cited Matsushita's multiplexers (104, 106, and 108) for selection purposes, however such a citation was not included in the latest Office Action sent out on 7/5/2006. The Examiner had initiated a rejection consisting of the combination of Matsushita and Miller for the

claim limitations of selecting an interface controller and had withdrawn the multiplexer selection as of 7/5/2006.

14. As per argument 4, the Examiner respectfully disagrees. The previous Office Action stated the associating of identified pins with that of the interface controller. In order to better understand the rejection the Examiner directs the Applicant to figures 3 through 5. The recognition decoder assists in the means of assigning pins identified (logical) with the connected I/O device (physical) via interface controller as explained in column 5, lines 65 – 67 and column 6, lines 1 – 44. Clearly from this citation one of ordinary skill in the art would recognize that assigning pins in a virtual/logical environment to a physical/connected environment would constitute associating pins.

15. As per argument 5, the Examiner respectfully disagrees. Applicant states the Examiner no long contends that the recognition decoder of Matsushita is analogous to the Applicant's interface controller. In the Office Action filed on 12/30/2005 the Examiner had referred to a recognition decoder to pertain to a "means" and not a single interface controller entity in the claim limitations. In view of the Applicant's Remarks received on 3/30/2006 the Examiner had noticed that the Applicant was unclear as to the previous rejection and required further explanation. In the Office Action filed on 7/5/2006 the Examiner had elaborated that the first Office Action had intended to reject the entire step consisting of "means for associating" and not the single element of an

interface controller. For the role of the recognition decoder please refer to the Examiners response to argument 4 above.

16. As per argument 6, the Examiner respectfully disagrees. Matsushita teaches a testing system in which pin assignment is utilized to handle a number variety of I/O devices. Matsushita teaches that an I/O device is present in figures 1 and 2, element 72. However Matsushita did not explicitly disclose that in order for an I/O device to be present and connected, a system would require an interface controller. The Examiner had cited Miller to elaborate on the connectivity of an I/O device with a system. Clearly one of ordinary skill in the art would recognize that Miller's teaching of how a device is connected to a system would be utilized in Matsushita's system of connected devices.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571) 272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

KIM HUYNH
SUPERVISORY PATENT EXAMINER

12/15/06